Design and Development of FPGA Softcore Processor Based TCP/IP Module for Real Time Computers in Nuclear Power Plants

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Abstract

An VME(Virtual Module Europa) bus based Real Time Computer's (RTC's) are being developed for Prototype Fast Breeder Reactor (PFBR) which is in an advanced stage of construction at Kalpakkam, where the RTC's have to communicate to the central process computer on the data collected from the field instrument and receive data from the central process computer. A Distributed Digital Control System (DDSC) architecture has been designed for this communication which is based on Transfer Communication Protocol/Internet Protocol (TCP/IP) over Ethernet.Currently the RTC's uses "Wiznet Module", a bought out chip which implements the TCP/IP stack in hardware. This project concentrates on the design and development of Field Programmable Gate Array (FPGA) based TCP/IP module that runs on Microblaze, a 32-bit softcore processor, to take care of the communication as that of Wiznet module. Advantage of switching over to FPGA based system are its reconfigurability, desired number of sockets, and the design is stable even if the FPGA's get obsolete.

Index Terms—VME bus, Real Time Computer's, Distributed Digital Control Systems, TCP/IP, Wiznet, Microblaze.

1.Introduction

The Prototype Fast Breeder Reactor (PFBR) is a 500MWe, sodium cooled, pool type, mixed oxide fuelled reactor having two secondary loops and is in the advanced stage of construction at Kalpakkam, India. It is first of its kind being built in India using Sodium as coolant and fast neutrons to sustain the nuclear reaction in commercial scale. Instrumentation & Control (I&C) systems are heart of any plant and they play vital role for safe and smooth plant operation. The information received from the field instruments are to be provided effectively and user friendly to the operator, so that he/she can make correct decisions and implement them in the shortest time possible. In nuclear power plants, I&C systems are used for protection, control, supervision and monitoring. The I&C systems of PFBR are categorized as safety critical, safety related and non nuclear safety systems (NNSs). Safety critical systems play a principal role in achievement of nuclear power plant safety. Safety related systems play a complementary role in achievement of nuclear power plant safety. Non nuclear safety systems play auxiliary or indirect role in achievement of nuclear power plant safety. The proper operation of safety related systems may avoid the need to initiate safety actions by safety critical system. In PFBR, the VME based Real Time Computer systems are deployed at different locations in the plant therebyachieving both functional and geographical distribution.

The I&C architecture is a three layered Distributed Digital control Systems. The bottom layer has field instruments which have are controlled by the Local Control Centers (LCC). The middle layer form the LCCs, where the RTCs are placed at different locations. The top layer has the process computers and the display stations in the control room which do the supervisory control by sending the control parameters in configuration data as prescribed by the operator.
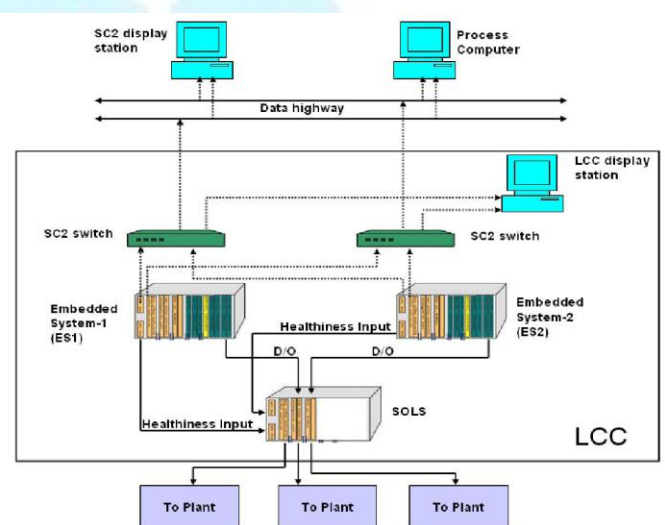

Fig-1 DDCS architecture

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Around 80 RTC systems are located at 11 local control centers of PFBR. Figure-1 shows the simplified architecture of Distributed Real Time Computers wherein RTC systems are placed at local control centers namely LCC1 and LCC2. In figure-1 ES1 refers to safety critical systems, ES2 refers to safety related systems and ES3 refers to non-nuclear safety systems. Each RTC system is connected to dual redundant switches present at LCC via category 5 UTP cable. Distance between LCCs and Control Room is considerably large. Hence fiber optic cables are used to connect switches across buildings.Safety critical and safety related core switches are connected to NNS core switches which are also termed as 'Plant Backbone'. All plant parameters can be monitored through NNS core switches. Process computers (PC) which are server class machines also connected to NNS core switches wherein all plant parameters are stored for historical data logging. Many operator display stations are connected to process computer where all plant parameters can be viewed. Dedicated display stations are connected to respective core switches in order to monitor the plant parameter in case of non availabilityof PC.

II.CurrentDesign

In current design, the RTCs uses Wiznet module, which is a hardcore processor, that takes care of TCP/IP communications.
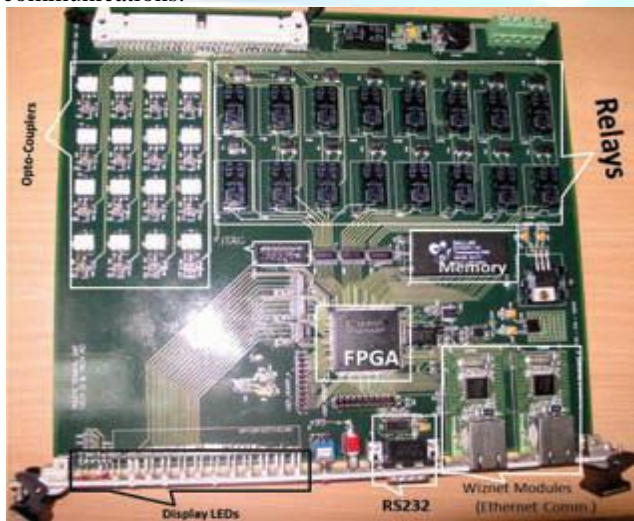

Fig-2 Current Model

III.Proposed Design

The current design has certain limitations such as obsoleteness, limited number of sockets (only four), unknown internal design. To overcome the limitations in the existing system, it has been proposed to design a FPGA based TCP/IP module, which takes care of the communication part, just similar to that of the Wiznet module. Some of the advantages in proposed design are FPGA reconfigurability, more number of sockets as desired, internal design is known, design is stable even if the FPGAs get obsolete.
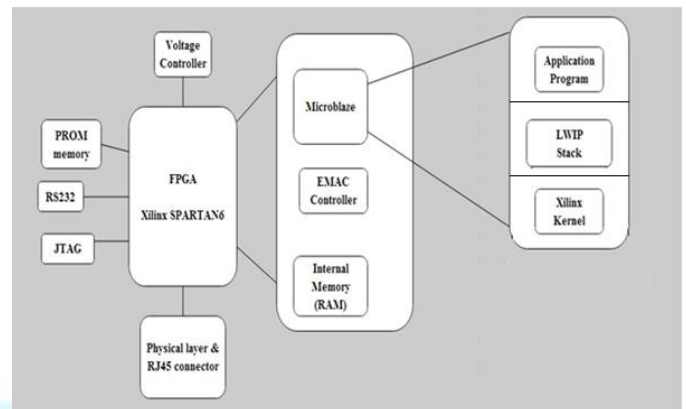

Fig-3 Proposed Block Diagram

The board consists of Xilinx SPARTAN-6 Field Programmable Gate Array connected with a voltage controller, external Programmable Read OnlyMemory(PROM), RS232 socket, JTAG download, RJ45 connector, Ethernet Media Access Controller (EMAC) and physical layer. A 5V power supply is given to the board. The configuration storage is volatile and must be reloaded whenever the FPGA is powered ON. Hence an external PROM is connected with the FPGA for configuration purpose. There are two mini USB jacks on the FPGA board. One of the USB connections connects the JTAG download and debug interface built into the SP605 FPGA. The other USB connection is a USB to RS232 bridge, in order for PC to map the USB port and the COM port. RJ45 connector is used for Ethernet connection that is responsible for the data transfer through the internet. The physical layer defines the means of transmitting raw bits over a physical link connecting network nodes. The bit stream may be grouped into code words or symbols and converted to a physical signal that is transmitted over a hardware transmission medium. The physical layer provides an electrical or mechanical interface to the transmission medium. Interfacing an FPGA based Microblaze system to an on-chip EMAC/PHY would reduce consume a smaller part of the targeted FPGA, and thus giving room for other on-chip peripherals or enable the use of a smaller sized FPGA. Employing a smaller FPGA is desirable since it would reduce power consumption and device price. Over the Microblaze, the xilkernel, LWIP and the application program are loaded in stack form. Xilkernel is a small light weight ease to use kernel. It works on Microblaze that is used to implement high level services such as networking and run applications using the services. Light weight IP is a widely used open source TCP/IP stack designed for embedded systems. The focus of the lwIP is to reduce the RAM usage while still having a full scale TCP/IP implementation. The application program is written in embedded C that loaded into the Microblaze.
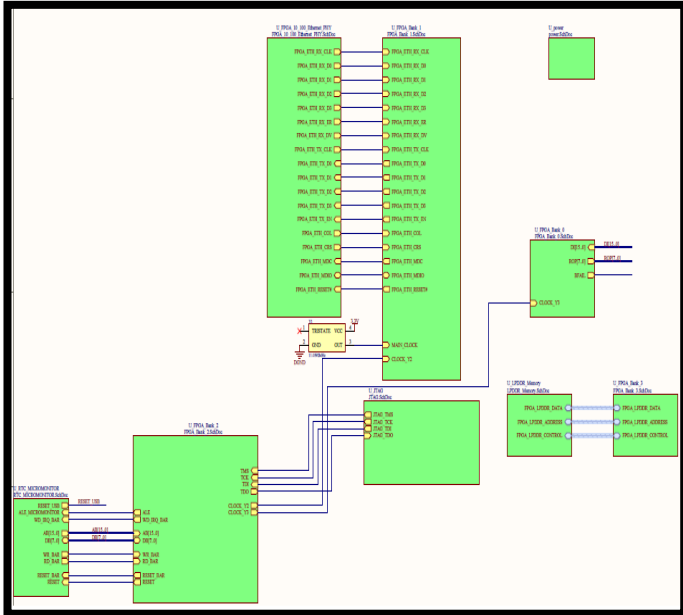
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I. Design and Network Module

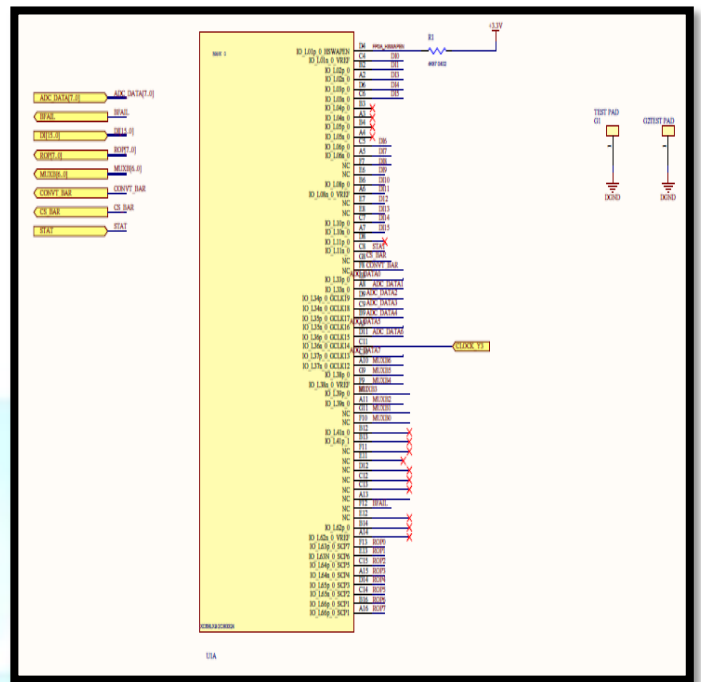*Fig.4 Schematic overview of proposed work done using Altium designer*

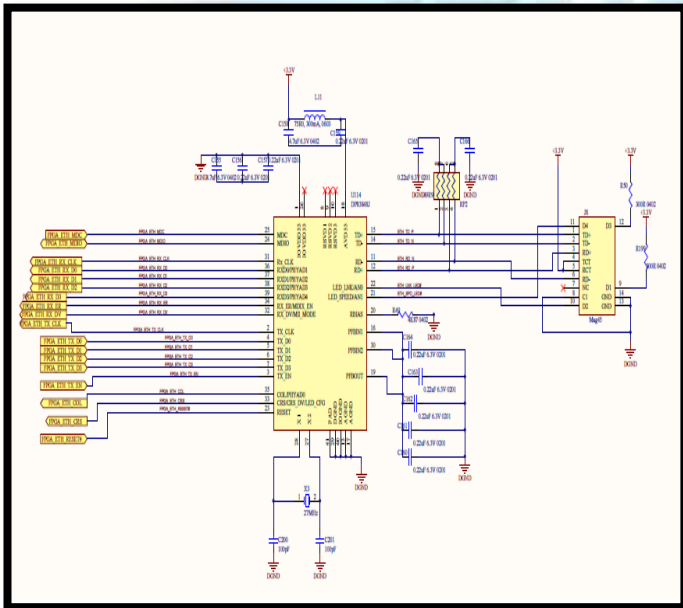*Fig.6 FPGA Bank0 connection drawn using Altium designer*

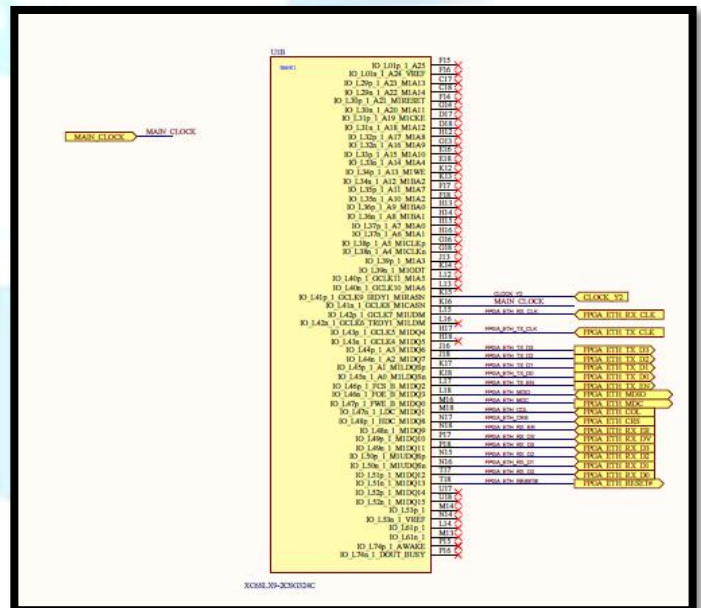*Fig.5 FPGA 10/100 Ethernet/PHY connection drawn using Altium designer*

Fig.7 FPGA Bank1 connection drawn using Altium designer

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Fig.8 FPGA Ban2 connection drawn using Altium designer

Fig.11 Power circuit connection drawn using Altium designer

Fig.9 FPGA Bank3 connection drawn using Altium designer

Fig.12 Real Time Clock Micro monitor circuit connection drawn using Altium designer

IV. Result and Discussion

Wiznet module (for TCP/IP communication) was used in the existing designs, which is becoming obsolete and its limitation of only four sockets makes us plan for its replacement with softcore EMAC controllers also downloaded to FPGA and a software TCP/IP stack implemented over an operating system ported to run on the softcore processor. Micrium provides such open source operating system and TCP/IP stacks for real time embedded applications. Experiments have been done successfully on a Xilinx SP605 development board and the design of universal RTU with RTOS has been done.

Fig.10 JTAG port connection drawn using Altium designer

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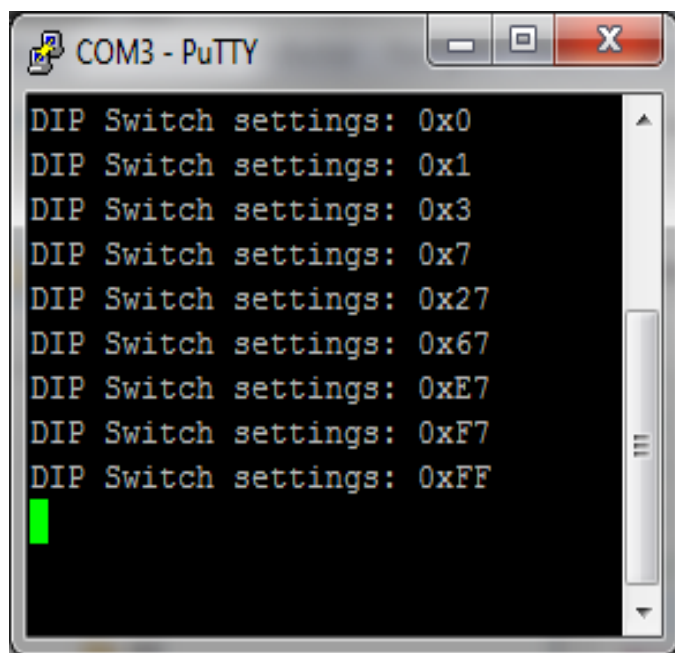ISSN: 2320 - 8791
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Fig-13Read dip switch using the microblaze

V.Conclusion

Once the proposed design is completed, in the manufactured product the TCP/IP stack(LWIP stack) is modified which is ported over Xilinx kernel running on the Microblaze. The whole setup is ported over the Xilinx Spartan FPGA and the full fledged testing for the capabilities of the new communication module will be done.

VI. Acknowledgement

VII.References

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